WHAT IS CLAIMED IS:

1. A transceiver, comprising:

a plurality of pads, wherein at least one of said plurality of pads is a programmable pad capable of supporting at least two standards;

a plurality of ports in communications with said plurality of pads, wherein one of said plurality of ports is a parallel port in communications with said programmable pad; and

means for enabling communications between a first port from said plurality of ports with a second port from said plurality of ports.

2. The transceiver of claim 1, wherein said at least two standards include XGMII data protocol, TBI data protocol, RTBI data protocol, HSTL electrical specification, SSTL electrical specification, or LVTTL electrical specification.

3. The transceiver of claim 1, wherein said programmable pad is programmable to operate as an input or an output.

4. The transceiver of claim 1, wherein said programmable pad is programmable to receive or send at least one of a data signal and a clock signal.

5. The transceiver of claim 1, wherein one of said plurality of ports is a serial port in communications with said programmable pad.

6. The transceiver of claim 5, wherein said serial port is XAUI.

7. The transceiver of claim 1, wherein one of said plurality of pads is a MDIO pad programmable to support at least two electrical specifications and at least two data protocols.

8. A transceiver, comprising:

a plurality of parallel ports;

a plurality of serial ports;

a bus connecting said parallel ports and said serial ports on a common substrate with said parallel ports and said serial ports; and

a plurality of programmable pads in communications with said plurality of parallel ports.

9. The transceiver of claim 8, wherein said bus is configured to have a ring shape.

10. The transceiver of claim 8, wherein said bus is configured to have a ring shape around a logic core.

11. The transceiver of clam 8, further comprising a packet bit error rate tester (BERT) connected to said bus, said packet BERT able to determine bit error rates of at least one of said multiple parallel ports and said multiple serial ports.

12. A transceiver, comprising:

a plurality of ports;

a bus connecting said plurality of ports on a common substrate;

a plurality of programmable pads in communications with said plurality of ports; and

a register for sending instructions to configure at least one of said programmable pads to comply with a specified data protocol and a specified electrical specification.

13. The transceiver of claim 12, further comprising:

a timing controller for modulating delay between input and output of at least one of said programmable pads.

14. The transceiver of claim 12, further comprising:

a timing register for sending instructions to adjust the delay between input and output of at least one of said programmable pads.

15. The transceiver of claim 12, further comprising:

an input controller for configuring at least one of said programmable pads to receive at least one of a data signal and a control signal.

16. The transceiver of claim 12, further comprising:

an output controller for configuring at least one of said programmable pads to send at least one of a data signal and a control signal.

17. The transceiver of claim 12, further comprising:

a testing register for sending a test message to measure leakage current from at least one of said programmable pads.

18. A method for programming a transceiver, comprising:

accessing protocol instructions that specify a data protocol;

executing said protocol instructions to configure a programmable pad disposed on the transceiver; and

sending or receiving data at said programmable pad in accordance with said data protocol and said electrical specification.

19. The method according to claim 18, further comprising:

sending an input control message to configure said programmable pad to receive at least one of data and a control message.

20. The method according to claim 18, further comprising:

sending an output control message to configure said programmable pad to send at least one of data and a control message.

21. The method according to claim 18, further comprising:

sending a test message to measure leakage current at said programmable pad.

22. The method according to claim 18, further comprising:

sending a delay control message to adjust the delay between input and output at said programmable pad.

23. The method according to claim 22, further comprising:

delaying data at said programmable pad for a fixed time interval;

sending said data to a destination external to said programmable pad upon expiration of said fixed time interval, wherein said delay control message determines said fixed time interval.

24. The method according to claim 22, further comprising:

delaying data in a buffer at said programmable pad for a fixed time interval;

sending said data to a second buffer or a destination external to said programmable pad upon expiration of said fixed time interval, wherein said delay control message determines whether said data is sent to said second buffer or said destination.

25. A transceiver, comprising:

protocol means for accessing protocol instructions that specify a data protocol; and

control logic for executing said protocol instructions to configure a programmable pad disposed on the transceiver, such that said

programmable pad is configured to send or receive data in accordance with said data protocol.

26. The transceiver of claim 25, further comprising:

input control means for instructing said programmable pad to receive at least one of data and a control message.

27. The transceiver of claim 25, further comprising:

output control means for instructing said programmable pad to send at least one of data and a control message.

28. The transceiver of claim 25, further comprising:

testing means for measuring leakage current at said programmable pad.

29. The transceiver of claim 25, further comprising:

timing means for adjusting the delay between input and output at said programmable pad.

30. The transceiver of claim 29, further comprising:

means for delaying data at said programmable pad for a fixed time interval; and

means for sending said data to a destination external to said programmable pad upon expiration of said fixed time interval, wherein said timing means determines said fixed time interval.